

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
:
QI XIANG :
:
Serial No.: Divisional of : Group Art Unit: To be assigned
Application No. 10/015,808 :
:
Filed: July 17, 2003 : Examiner: To be assigned
:
For: CMOS WITH STRAINED SILICON CHANNEL NMOS AND SILICON GERMANIUM
CHANNEL PMOS

TRANSMITTAL OF FORMAL DRAWINGS

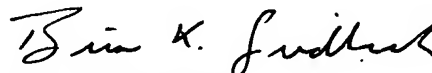
Mail Stop NEW APPLICATIONS/FORMAL DRAWINGS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Three (3) sheets of formal drawings are submitted herewith as filed in parent application
Serial No. 10/015,808. These drawings were filed in the parent application on May 9, 2002. It is
believed that the requirements under 37 CFR 1.84 for this application have been met.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Brian K. Seidleck
Registration No. 51,321

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 BKS:BD
Facsimile: (202) 756-8087
Date: July 17, 2003